OIPE JC18 JUN 22 2001 PATENT & TRADEMARK OFFICE

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Attorney Docket Number	**40704/PYI/F179**
Application Number	09/851,708
Filing Date	May 8, 2001
Applicant(s)	Indradeep Ghosh
Group Art Unit	
Examiner Name	Not Yet Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
RSD	5,513,123	04/1996	Dey et al.	364	489	
RSD	5,602,856	02/1997	Teramoto	371	27	
RSD	5,615,124	03/1997	Hemmi et al.	364	488	
RSD	5,625,630	04/1997	Abramovici et al.	371	22.1	
RSD	5,696,771	12/1997	Beausang et al.	371	22.3	
RSD	5,875,196	02/1999	Chakradhar et al.	371	22.1	
RSD	5,883,809	03/1999	Sullivan et al.	364	489	
RSD	5,933,356	08/1999	Rostoker et al.	364	489	
RSD	5,991,523	11/1999	Williams et al.	395	500.19	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY OR PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS

EXAMINER INITIALS	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSD	SANDHYA SESHADRI and MICHAEL S. HSIAO, "An Integrated Approach to Behavioral-Level Design-For-Testability Using Value-Range and Variable Testability Techniques", International Test Conference, 1999, pp. 858-867.
RSD	ALBRECHT P. STROELE, "Synthesis for Arithmetic Built-In Self-Test", 18th IEEE VLSI Test Symposium, Montreal, Canada, May 2000, pp. 165-170.
RSD	ALBRECHT P. STROELE, "Synthesizing Data Paths with Arithmetic Self-Test", IEEE International Symposium on Circuits and Systems (ISCAS), Geneva, Switzerland, May 2000, pp. II-45-48.
RSD	MARK C. HANSEN and JOHN P. HAYES, "High-Level Test Generation using Physically-Induced Faults", VLSI Test Symposium Paper, May 1995, pp. 1-9.

EXAMINER SIGNATURE	R. Stephen Williams	DATE CONSIDERED	1/23/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449	Attorney Docket Number	40704/PYI/F179
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	09/851,708
	Filing Date	May 8, 2001
	Applicant(s)	Indradeep Ghosh
	Group Art Unit	
(use as many sheets as necessary)	Examiner Name	Not Yet Assigned

OIPE JC03 JUN 22 2001 PATENT & TRADEMARK OFFICE

OTHER DOCUMENTS	
EXAMINER INITIALS	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSD	JAAN RAIK, "Hierarchical Test Generation Based on Alternative Graph Models", Computer Engineering and Diagnostics Department of the Institute of Computer Engineering, April 1997, pp. 1-44, Tallinn Technical University, Estonia.
RSD	INDRADEEP GHOSH, ANAND RAGHUNATHAN and NIRAJ K. JHA, "Design for Hierarchical Testability of RTL Circuits Obtained by Behavioral Synthesis", IEEE International Conference on Computer Design, 1995, pp. 1-27.
RSD	INDRADEEP GHOSH, ANAND RAGHUNATHAN, and NIRAJ K. JHA, "A Design for Testability Technique for RTL Circuits Using Control/Data Flow Extraction", In Proc. IEEE International Conference on Computer-Aided Design, 1996.
RSD	INDRADEEP GHOSH, ANAND RAGHUNATHAN, and NIRAJ K. JHA, "Hierarchical Test Generation and Design for Testability of ASPPs and ASIPs", ACM, Inc., DAC 97, Anaheim, California.
RSD	SILVIA CHIUSANO, FULVIO CORNO, PAOLO PRINETTO, "RT-level TPG Exploiting High-Level Synthesis Information, 17th IEEE VLSI Test Symposium, April 1999.
RSD	YIORGOS MAKRIS and ALEX ORAILOĞLU, "Property-Based Testability Analysis for Hierarchical RTL Designs", In Proceedings of the IEEE International Conference on Electronics Circuits and Systems, pp. 1089-1092, 1999.
RSD	INDRADEEP GHOSH, NIRAJ K. JHA and SUDIPTA BHAWMIK, "A BIST Scheme for RTL Circuits Based on Symbolic Testability Analysis", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, January 2000.

EXAMINER SIGNATURE	R Stephen Davine	DATE CONSIDERED	1/23/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

COPY OF PAPERS
ORIGINALLY FILED

OIPE
APR 29 2002
PATENT & TRADEMARK OFFICE

FORM PTO/SB/08A/B (10-01) Substitute for PTO-1449A/B **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (use as many sheets as necessary)		
	Attorney Docket Numb r	**40704/DMC/F179**
	Application Number	09/851,708
	Filing Date	May 8, 2001
	Applicant(s)	Indradeep Ghosh
	Group Art Unit	2858
	Examiner Name	To Be Assigned

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSD		Farzan FALLAH, et al., "Simulation Vector Generation from HDL Descriptions for Observability-Enhanced Statement Coverage", 36th Design Automation Conference, New Orleans, 6 pgs, (June 1999)
RSD		Abhijit GHOSH, et al., "Sequential Test Generation and Synthesis for Testability at the Register-Transfer and Logic Levels", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 12, No. 5, pp 579-598 (May 1993)

RECEIVED
MAY 09 2002
Technology Center 2100

EXAMINER SIGNATURE	R. Stephen Dildine	DATE CONSIDERED	1/23/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DMC/rmw
RMW IRV1053919.1-*-4/16/02 4:39 PM

RECEIVED
MAY -2 2002
TC 2800 MAIL ROOM

OIPE JC42 APR 29 2002 PATENT & TRADEMARK OFFICE

COPY OF PAPERS ORIGINALLY FILED

FORM PTO/SB/08A/B (10-01)
Substitute for PTO-1449A/B

INFORMATION DISCLOSURE

STATEMENT BY APPLICANT

(use as many sheets as necessary)

Attorney Docket Numb r	40704/DMC/F179
Application Number	09/851,708
Filing Date	May 8, 2001
Applicant(s)	Indradeep Ghosh
Group Art Unit	2858
Examiner Name	To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - kind code[2] - (If known)	PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE

RECEIVED
MAY 0 9 2002
Technology Center 2100

RECEIVED
MAY - 2 2002
TC 2800 MAIL ROOM

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (Y)

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSO		Viraphol CHAIYAKUL, et al., "High-Level Transformations for Minimizing Syntactic Variances", 30th ACM/IEEE Design Automation Conference, pp 413-418 (1993)
RSO		Fulvio CORNO, et al., "Testability Analysis and ATPG on Behavorial RT-Level VHDL", IEEE, International Test Conference, Paper 30.4, pp 753-759 (1997)
RSO		Sujit DEY, et al., "Non-Scan Design-For-Testability of RT-Level Data Paths", ACM, 11 pages (1994)

EXAMINER SIGNATURE	R. Stephen Dildine	DATE CONSIDERED	1/23/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

APR 12 2002
PATENT & TRADEMARK OFFICE
JO190

#3

FORM PTO/SB/08A/B (10-01) Substitute for PTO-1449A/B	Attorney Docket Number	40704/PYI/F179
INFORMATION DISCLOSURE	Application Number	09/851,708
	Filing Date	May 8, 2001
STATEMENT BY APPLICANT	Applicant(s)	Indradeep Ghosh
	Group Art Unit	2858
(use as many sheets as necessary)	Examiner Name	To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - kind code[2]- (If known)	PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE

RECEIVED
APR 25 2002
Technology Center 2100

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4]- Kind Code[5] (If known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSD		LAMPORT, L., "The Temporal Logic of Actions", Revised Version of SRC Research Report 79 to appear in ACM Transactions on Programming Languages and Systems, (19 pages) April 1994.
RSD		GHOSH, S., "Test Compaction at the Register Transfer or Behavior level", Project Report, ELE 466: Digital System Testing, Dept. of Electrical Engineering, Princeton University, Princeton, NJ (8 pgs), 1994.
RSD		K. Chakrabarty, R. Mukherjee and A. Exnicios, "Synthesis of Transparent Circuits for Hierarchical and System-on-a-Chip Test", Proc. IEEE International Conference on VLSI Design, pp. 431-436, Bangalore, India, January 2001.

EXAMINER SIGNATURE	R Stephen Davis	DATE CONSIDERED	1/23/2004

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.